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Transformer-less single-phase unified power quality conditioner of no circulating current

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Abstract: This study presents a unified current-source power quality conditioner of inherent no circulating current. It is formed of a three-leg current-source ac/ac converter and a specially designed small size dc-link. Owing to the transformers-less feature and small size dc-link, the proposed topology has the benefit of high power density. In addition, without the need to address the circulating current issue, it is easier to design the controllers and filters for the circulating current compared to other existing transformer-less unified power quality conditioners. To handle the harmonic currents compensation, voltage sags/swells elimination, power factor correction simultaneously and achieve excellent dynamic and steady-state performance, a direct control method based on an extended repetitive disturbance observer is proposed. Detailed analysis of topology and operation principles is given, followed by the modulation scheme and the developed control method. Simulations and experimental results are presented to verify the effectiveness of the conditioner.

1 Introduction

Nowadays the wide use of non-linear power electronic loads gives rise to some serious power quality (PQ) problems, such as poor power factor, voltage sags/swells, and harmonics. Meanwhile, developments in digital electronics, communication and process control have increased the number of sensitive loads that require ideal power supply [1–3]. Thus, PQ enhancement devices should be installed to ensure the supply of high-quality power.

A lot of power electronic devices have been adopted to improve PQ. Generally, an active power filter (APF) is used to handle the current-related PQ problems, while dynamic voltage restorer (DVR) is preferred to tackle the voltage-related PQ problems [4, 5]. Unified PQ conditioner (UPQC), as the integration of an APF and a DVR sharing a common dc-link [6–23], can deal with both current and voltage-type of PQ issues, simultaneously. Specifically, it can regulate load voltage, mitigate voltage transients, eliminate source current harmonics, and correct source power factor over a wide operating range.

The classical configuration of UPQC in a single-phase system usually has four legs and an isolation transformer [9–11]. Apart from a large number of active switches, the cost and size associated with the transformer make such UPQC undesirable in office and home environment applications. To remove the bulky isolation transformer, a transformer-less single-phase universal APF is proposed in [13]. However, it still needs eight active switches. Moreover, a circulating current issue exists in it, which will decrease the overall efficiency and cause instability if it is not well controlled. The three-leg [14, 15] and two-leg UPQCs [16–18] are two more cost-effective configurations, which do not have circulating current issues. The two-leg UPQC consists of two half-bridge inverters with or without an isolation transformer. Though the number of switches is minimum, the voltage rating is doubled. Moreover, two dc-link capacitors are needed and their voltages should be balanced. The three-leg UPQC is considered to be a preferable choice with a superior compensation performance in low-cost low-power applications, as less number of switches and no isolation transformer are employed. Additionally, the coupling effects between the APF and DVR introduced by the common leg can be well addressed through the space vector modulation [15]. However, it still suffers the limitation of low power density as a bulky dc-link is needed to provide sufficient voltage sag/swell ride-through capacity.

A single-phase UPQC of inherent no circulating current is proposed in this study, which consists of three current-source legs and a hybrid dc-link. One distinct difference between the other existing ones is that it has two small passive elements in the dc-link (a capacitor and an inductor). The capacitor is used to buffer the power difference between the input and the output, and the inductor is applied to filter the high-frequency switching harmonics. As a result, a stable dc-link current is obtained without using the bulky passive elements, which are usually found in the traditional UPQC topologies. Therefore, it is a high power density UPQC topology. Furthermore, the proposed converter does not have to address the circulating current issue which is an annoying problem in most existing transformer-less topologies.

In addition, to obtain a good compensation performance for various PQ problems, a direct control strategy based on extended repetitive disturbance observer (ERDO) is proposed for the conditioner. The load voltage and source current are directly controlled well without harmonic extractors. Therefore, the detrimental effects caused by the harmonic extractor are eliminated. What is more, a cost reduction is also achieved, as the load current is observed by the ERDO in place of the hardware sensor.

The remainder of this paper is organised as follows: Section 2 introduces the circuit configuration of the converter. In Section 3, the corresponding modulation schemes for both three legs and hybrid dc-link are presented. The modelling and control strategy are given in Section 4. Simulation and experimental results are presented in Section 5. Finally, the main points of this paper are summarised in Section 6.

2 Circuit configuration and operation principles

2.1 Circuit configuration

Fig. 1 shows the topology of the proposed UPQC. It consists of an input filter (L_p, C_i), an output filter C_o, three switching bridge legs (*A, B, C*), and a hybrid dc-link composed of an inductor L_d and a power buffer circuit. Bridge legs (*A, B*) form a shunt APF, which provides current compensation, while bridge legs (*B, C*) constitute

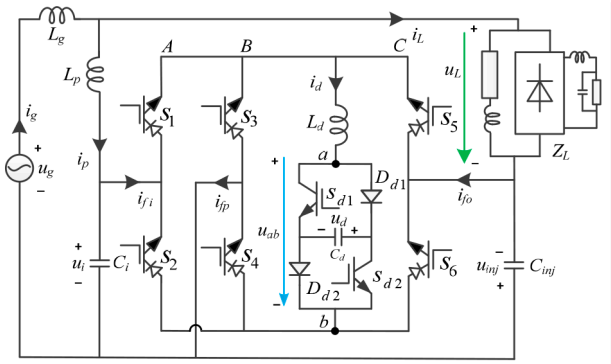

Fig. 1 *Proposed UPQC topology*

Table 1 Switching combinations and corresponding current vectors

Switching states (S_1–S_6)	Vectors	I_{fi}	I_{fo}
100100	$\boldsymbol{I}_1 = I_d$	I_d	0
000110	$\boldsymbol{I}_2 = I_d e^{j(\pi/2)}$	0	I_d
010010	$\boldsymbol{I}_3 = \sqrt{2} I_d e^{j(3\pi/4)}$	$-I_d$	I_d
011000	$\boldsymbol{I}_4 = I_d e^{j\pi}$	I_d	0
001001	$\boldsymbol{I}_5 = I_d e^{j(3\pi/2)}$	0	$-I_d$
100001	$\boldsymbol{I}_6 = \sqrt{2} I_d e^{j(7\pi/4)}$	I_d	$-I_d$
110000/001100/000011	$\boldsymbol{I}_{7,8,9} = \boldsymbol{I}_0 = 0$	0	0

a DVR to provide voltage compensation. The power buffer circuit, composed of two active switches (S_{d1}, S_{d2}), two diodes (D_{d1}, D_{d2}) and a film capacitor C_d, is used to buffer the power difference between the source and the load. L_g represents the impedance of the line and Z_L represents a non-linear load.

2.2 Operation principles

The proposed UPQC, combined with the proposed control method, is able to modify the load voltage and the current drained from the grid. From Fig. 1, assuming the line impedance L_g is pretty small and the voltage across it is approximately equal to zero during steady state, the load voltage u_L is expressed as

$$u_L = u_{inj} + u_g \tag{1}$$

As seen, to mitigate voltage sags/swells, a required compensation voltage u_{inj} can be generated by the DVR. Therefore, by adjusting the voltage u_{inj}, a steady load voltage u_L is ensured regardless of the variation of the source voltage u_g.

Source current i_g is comprised of the compensation current i_p and the load current i_L, given as

$$i_g = i_p + i_L \tag{2}$$

From (2) the harmonic and reactive currents generated by non-linear loads can be compensated by modifying the APF current i_p. Therefore, the current drained from the grid is harmonic free and in phase with the source voltage, i.e. the power factor correction is achieved.

3 Modulation scheme

3.1 Space vector modulation strategy for UPQC

A space vector modulation strategy for the proposed UPQC is adopted. Treating the input current (i_{fi}) and the output current (i_{fo}) of the UPQC as a unit, then a current vector is defined as

$$\boldsymbol{I}_n = i_{fi} + j \cdot i_{fo} \tag{3}$$

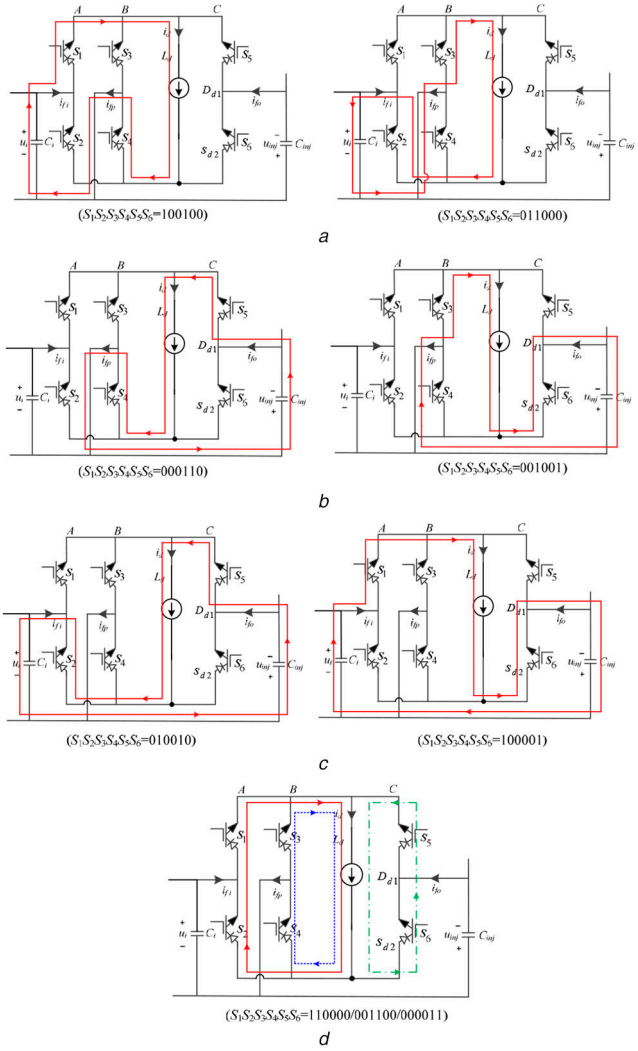

Fig. 2 *Switching states for the three switching arm*
(a) Synthesising the current i_{fi}, ***(b)*** Synthesising the current i_{fo}, ***(c)*** Synthesising the currents i_{fi} and i_{fo}, ***(d)*** Freewheeling states

Note that the current i_{fp} is equal to i_{fi}–i_{fo}.

There are nine possible switching combinations for the proposed UPQC in Fig. 1. The nine switching combinations correspond to nine basic current vectors shown in Table 1, where I_d is the steady-state dc-link current. As seen, there are six valid vectors and three zero vectors. The current path of each current vector is described in Fig. 2 and the dc link is replaced with a current source. Fig. 3 shows the current vectors in the complex plane, which is divided into six sectors with the sector number from $n = 1$ to $n = 6$. $I_{ref} = i_{fi}^* + j \cdot i_{fo}^*$ represents the reference current to be synthesised within one switching period T_s.

According to the space vector synthesis principle described in [24], $\boldsymbol{I}_{ref}$ can be synthesised by two adjacent valid vectors in sector n and a zero vector. Then, $\boldsymbol{I}_{ref}$ is rewritten as

$$\boldsymbol{I}_{ref} = \boldsymbol{I}_n \frac{t_n}{T_s} + \boldsymbol{I}_{n+1} \frac{t_{n+1}}{T_s} + \boldsymbol{I}_0 \frac{t_0}{T_s} \tag{4}$$

where t_n, t_{n+1}, and t_0 are the time weights for each vector during a switching period T_s and satisfy the following relation:

$$t_n + t_{n+1} + t_0 = T_s \tag{5}$$

In each sector, the zero vector is selected so that the total switching times are minimal. The selected zero vector and time weights of the current vectors in each sector are summarised in Table 2.

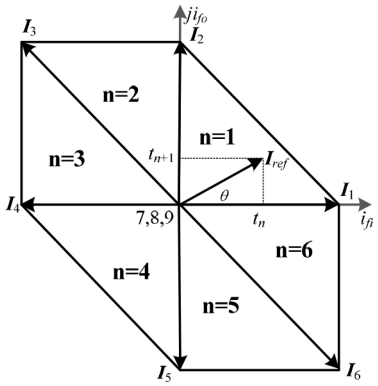

Fig. 3 *Current vectors diagram of the UPQC*

Table 2 Time weights of the current vector in each sector

Sector	t_n	t_{n+1}	Selected zero vector
1,4	$\text{abs}(i_{\text{fi}}^*)\cdot\frac{T_\text{s}}{i_\text{d}}$	$\text{abs}(i_{\text{fo}}^*)\cdot\frac{T_\text{s}}{i_\text{d}}$	9
2,5	$[\text{abs}(i_{\text{fo}}^*)-\text{abs}(i_{\text{fi}}^*)]\cdot\frac{T_\text{s}}{i_\text{d}}$	$\text{abs}(i_{\text{fi}}^*)\cdot\frac{T_\text{s}}{i_\text{d}}$	8
3,6	$\text{abs}(i_{\text{fo}}^*)\cdot\frac{T_\text{s}}{i_\text{d}}$	$[\text{abs}(i_{\text{fi}}^*)-\text{abs}(i_{\text{fo}}^*)]\cdot\frac{T_\text{s}}{i_\text{d}}$	7

Table 3 Time weights of switches S_{d1} and S_{d2}

Cases	S_{d1}	S_{d2}
$u_{ab}^*>0$	$\left(1-\frac{u_{ab}^*}{u_\text{d}}\right)\cdot T_\text{s}$	0
$u_{ab}^*\le 0$	T_s	$-\frac{u_{ab}^*}{u_\text{d}}\cdot T_\text{s}$

3.2 Modulation strategy for the power buffer circuit

The power buffer circuit is designed to keep the voltage-second balance of the dc-link inductor. Referring to Fig. 1, C_d in the power buffer circuit will be charged when both switches S_{d1} and S_{d2} are turned-off and discharged when they are turned-on. The on-time of switches S_{d1} and S_{d2} during one switching period is summarised in Table 3, where u_d is the terminal voltage of C_d, u_{ab} is the equivalent voltage provided by the power buffer circuit and $u{*}\ ab$ is the reference value of u_{ab}.

4 Modelling and control

4.1 Modelling of UPQC

According to Fig. 1, the model of the shunt APF is formulated as the following based on elementary circuit theory:

$$L_\text{g}\frac{\text{d}i_\text{g}}{\text{d}t}=u_\text{g}-u_\text{L}+u_{\text{inj}} \tag{6}$$

$$L_\text{p}\frac{\text{d}i_\text{p}}{\text{d}t}=u_\text{L}-u_i-u_{\text{inj}} \tag{7}$$

$$C_\text{i}\frac{\text{d}u_\text{i}}{\text{d}t}=i_\text{p}-i_{\text{fi}} \tag{8}$$

where u_i is the voltage of filter capacitor C_i.

Similarly, the model of the DVR can be formulated as

$$C_{\text{inj}}\frac{\text{d}u_{\text{inj}}}{\text{d}t}=i_{\text{fo}}-i_\text{L} \tag{9}$$

With regard to the hybrid dc-link, the dynamic differential equations of the inductor current and the capacitor voltage are

$$L_\text{d}\frac{\text{d}i_\text{d}}{\text{d}t}=\frac{u_i i_{\text{fi}}^*}{i_\text{d}}-\frac{u_{\text{inj}}i_{\text{fo}}^*}{i_\text{d}}-u_{ab} \tag{10}$$

$$C_\text{d}\frac{\text{d}u_\text{d}}{\text{d}t}=-\left|\frac{u_{ab}^*}{u_d}\right|\cdot i_\text{d} \tag{11}$$

4.2 Controller design

Lots of control methods have been proposed for UPQCs [3, 8, 12, 19, 20]. They can be broadly separated into two categories: the direct control methods [8, 12] and the indirect control methods [3, 19, 20, 21]. The indirect control methods usually need harmonic extractors and the control performance relies on the accuracy of harmonic extractors. The direct control methods can regulate the load voltage and source current without harmonic extractor, thus can achieve better compensation performance. In this study, a direct control strategy based on ERDO is presented. All the unknown disturbances are taken together as a single one and estimated. Then, the observer design can be simplified dramatically. Besides, the load current sensor is saved because the load current information is included in the observer.

4.2.1 Load voltage regulation based on ERDO: The load voltage is regulated by modifying the compensation voltage u_{inj} generated by the DVR. Based on (9) and the derivative of (1) the load voltage dynamic equation is formulated as

$$C_{\text{inj}}\frac{\text{d}u_\text{L}}{\text{d}t}=i_{\text{fo}}+C_{\text{inj}}\frac{\text{d}u_\text{g}}{\text{d}t}-i_\text{L} \tag{12}$$

For simplicity, (12) is rewritten as

$$\frac{\text{d}u_\text{L}}{\text{d}t}=\frac{i_{\text{fo}}}{C_{\text{inj}}}+w \tag{13}$$

where $w=(\dot{u}_\text{g}-i_\text{L}/C_{\text{inj}})$, can be viewed as the total disturbance. Since i_L and $\dot{u}_\text{g}$ are both periodic disturbances, w is also periodical. Assume the period of w is T, then

$$w(t)=w(t-T) \tag{14}$$

Inspired by the active disturbance rejection control idea [25, 26], an ERDO is proposed to estimate the disturbance in real time. w is viewed as an extended state variable. Once it is observed, it will be actively compensated through feedforward control. Similar to the structure of the Luenberger observer, the ERDO is designed as

$$\frac{\text{d}\hat{u}_\text{L}(t)}{\text{d}t}=\frac{i_{\text{fo}}(t)}{C_{\text{inj}}}+\hat{w}(t)+k_1\big(u_\text{L}(t)-\hat{u}_\text{L}(t)\big) \tag{15}$$

$$\hat{w}(t)=\frac{1}{\lambda}\hat{w}(t-T)+k_2[u_\text{L}(t)-\hat{u}_\text{L}(t)] \tag{16}$$

where k_1 and k_2 are the observer gains and λ is the forgetting factor to guarantee stability. Suppose $e=u_\text{L}-\hat{u}_\text{L}$, $\tilde{w}=w-\hat{w}$, then the error dynamic equations of the system are given by

$$\frac{\text{d}e(t)}{\text{d}t}=\tilde{w}(t)-k_1e(t) \tag{17}$$

$$\tilde{w}(t)=\frac{1}{\lambda}\cdot\tilde{w}(t)-k_2e(t)+\frac{\lambda-1}{\lambda}w(t) \tag{18}$$

To prove the stability of the control system, we choose a Lyapunov function candidate as

$$V(e,\tilde{w}) = \frac{1}{2}e^2(t) + \int_{t-T}^{t} \tilde{w}^2(\tau)\mathrm{d}\tau \tag{19}$$

Then

$$\begin{aligned}\dot{V}(e,\tilde{w}) &= (1-\lambda^2)\tilde{w}^2 - (k_1+\lambda^2 k_2^2)e^2 - (2\lambda^2 k_2 - 1)e\tilde{w} \\ &\quad +2\lambda(\lambda-1)w\tilde{w} + 2\lambda(\lambda-1)we - (\lambda-1)^2 w^2 \\ &\le (1-\lambda)\tilde{w}^2 - (2\lambda^2 k_2 - 1)e\tilde{w} - [(k_2^2-1)\lambda^2 + \lambda \\ &\quad +k_1]e^2 + (\lambda^2-1)w^2 \\ &\le -(\lambda-0.5)\tilde{w}^2 - [(k_2^2+2k_2-1)\lambda^2 + \lambda + k_1 - 1]e^2 \\ &\quad +(k_2\lambda+1)(\lambda-1)w^2\end{aligned} \tag{20}$$

Since the periodic disturbance w is bounded, there is a constant M such that $(\lambda^2-1)w^2 \le M$. From the input-state stability criterion, k_1 and k_2 should satisfy the inequality

$$(k_2^2+2k_2-1)\lambda^2 + \lambda + k_1 - 1 > 0 \tag{21}$$

Then the control law of the load voltage controller is designed as

$$i_{\mathrm{fo}}^* = u_1(\hat{w}, u_{\mathrm{L}}) = C_{\mathrm{inj}}\left[k_{\mathrm{L}}(u_{\mathrm{L}}^* - u_{\mathrm{L}}) - \hat{w}\right] \tag{22}$$

where k_{L} is the control parameter and $u*$ L denotes the reference of load voltage.

4.2.2 Source current regulation based on ERDO: The task of the APF is to compensate for the reactive and harmonic components of load current and regulate the average value of the capacitor voltage u_{d} during normal and disturbance conditions.

To maintain the dc component of the capacitor voltage $\bar{u}_{\mathrm{d}}$ at a given voltage level, a capacitor voltage control outer loop is adopted, as shown in Fig. 4. Since the dc-link inductor L_{d} is small and the energy stored in it is negligible compared with that of the capacitor C_{d}. According to the power balance principle, we have

$$C_{\mathrm{d}}\frac{\mathrm{d}u_{\mathrm{d}}^2}{\mathrm{d}t} = 2(p_{\mathrm{in}} - p_{\mathrm{out}}) \tag{23}$$

The right side of (23) is a periodic function. The periodic averaging method is used to facilitate the control design. The average differential equation is written as

$$C_{\mathrm{d}}\frac{\mathrm{d}\bar{x}}{\mathrm{d}t} = U_{\mathrm{g}}I_{\mathrm{g}}\cos(\varphi_i) - \bar{p}_{\mathrm{out}} \tag{24}$$

where $\bar{x} = \bar{u}_{\mathrm{d}}^2$ is obtained by a moving average filter and can be described in the continuous-time domain by

$$\bar{x} = \frac{1}{T_\omega}\int_{t-T_\omega}^{t} x(t)\mathrm{d}t\,. \tag{25}$$

In (24), T_ω is the window length, which is selected to be the period of u_{d} in this study.

From (24), I_{g} can be selected as the control variable to maintain the dc component of the capacitor voltage u_{d}. A proportional–integral (PI) controller is adopted to control the average value of u_{d}, as (24) is a linear first-order differential equation.

For the power factor and harmonic current control, the instantaneous reference source current i^*_{g} must be synchronised with voltage u_{g}. This is performed by a phase-locked loop, as shown in Fig. 4. Then

$$i_{\mathrm{g}}^* = I_{\mathrm{g}}^*\cos(\omega_i \cdot t) \tag{26}$$

Based on (2), (6) and (7), the grid current dynamic equation is expressed as

$$(L_{\mathrm{p}} + L_{\mathrm{g}})\frac{\mathrm{d}i_{\mathrm{g}}}{\mathrm{d}t} = L_{\mathrm{p}}\frac{\mathrm{d}i_{\mathrm{L}}}{\mathrm{d}t} + u_{\mathrm{g}} - u_i \tag{27}$$

$$C_i\frac{\mathrm{d}u_i}{\mathrm{d}t} = i_{\mathrm{g}} - i_{\mathrm{L}} - i_{\mathrm{fi}} \tag{28}$$

Let $z_1 = i_{\mathrm{g}}$, according to (27) and (28) the source current dynamic equations can be rewritten as

$$\frac{\mathrm{d}z_1}{\mathrm{d}t} = z_2 \tag{29}$$

$$\frac{\mathrm{d}z_2}{\mathrm{d}t} = \frac{i_{\mathrm{fi}}}{(L_{\mathrm{p}}+L_{\mathrm{g}})C_i} + \xi \tag{30}$$

where
$\xi = (1/(L_{\mathrm{p}}+L_{\mathrm{g}}))\dot{u}_{\mathrm{g}} + (L_{\mathrm{p}}/(L_{\mathrm{p}}+L_{\mathrm{g}}))\ddot{i}_{\mathrm{L}} - (1/C_{\mathrm{i}}(L_{\mathrm{p}}+L_{\mathrm{g}}))(i_{\mathrm{g}} - i_{\mathrm{L}})$ represents the unknown disturbance which is assumed to be bounded, and $\xi(t) = \xi(t-T_1)$. Using $\hat{z}_1$, $\hat{z}_2$, and $\hat{\xi}$ to estimate z_1, z_2, and ξ, respectively, the ERDO is designed as

$$\frac{\mathrm{d}\hat{z}_1(t)}{\mathrm{d}t} = \hat{z}_2(t) + \beta_1(z_1(t) - \hat{z}_1(t)) \tag{31}$$

$$\frac{\mathrm{d}\hat{z}_2(t)}{\mathrm{d}t} = -\frac{i_{\mathrm{fi}}(t)}{(L_{\mathrm{p}}+L_{\mathrm{g}})C_{\mathrm{i}}} + \hat{\xi}(t) + \beta_2(z_1(t) - \hat{z}_1(t)) \tag{32}$$

$$\hat{\xi}(t) = \frac{1}{\lambda}\hat{\xi}(t-T_1) + \beta_3(z_1(t) - \hat{z}_1(t)) \tag{33}$$

where β_1, β_3, and β_3 are the observer gains, which should be tuned properly. Suppose $e_1 = z_1 - \hat{z}_1$, $e_2 = z_2 - \hat{z}_2$, and $\tilde{\xi} = \xi - \hat{\xi}$, then the error dynamic equations of the system are given by

$$\frac{\mathrm{d}e_1(t)}{\mathrm{d}t} = e_2(t) - \beta_1 e_1(t) \tag{34}$$

$$\frac{\mathrm{d}e_2(t)}{\mathrm{d}t} = \tilde{\xi}(t) - \beta_2 e_1(t) \tag{35}$$

$$\tilde{\xi}(t) = \frac{1}{\lambda}\cdot\tilde{\xi}(t-T_1) - \beta_3 e_1(t) + \frac{\lambda-1}{\lambda}\xi(t) \tag{36}$$

Similar to (19), choosing a Lyapunov function candidate as

$$V_1(e_1, e_2, \tilde{\xi}) = \frac{1}{2}[e_1^2(t) + e_2^2(t)] + \int_{t-T_1}^{t} \tilde{\xi}^2(\tau)\mathrm{d}\tau \tag{37}$$

Then, β_1, β_2, and β_2 can be determined by letting $\dot{V}_1 \le 0$. Based on the observed information, the source current regulation controller is designed as

$$i_{\mathrm{fi}}^* = u_2(\hat{\zeta}, \hat{z}_1, \hat{z}_2) = (L_{\mathrm{p}}+L_{\mathrm{g}})C_{\mathrm{i}}\left[k_{\mathrm{g}}(i_{\mathrm{g}}^* - i_{\mathrm{g}}) - k_{\mathrm{d}}\hat{z}_2 - \hat{\xi}\right] \tag{38}$$

where k_{g} and k_{d} are the control parameters.

4.2.3 Dc-link inductor current regulation: The dc-link current will appear low-frequency oscillation in the presence of power difference between source and loads. From (10), u_{ab} could be used to regulate the dc-link current i_{d}. For simplicity, a PI compensator is employed. Also, the control input u_{ab} is designed as

$$u_{ab}^* = \left(k_{\mathrm{p}} + \frac{k_{\mathrm{i}}}{s}\right)(i_{\mathrm{d}}^* - i_{\mathrm{d}}) + u_{\mathrm{ri}} \tag{39}$$

where $u_{\mathrm{ri}} = 1/i_{\mathrm{d}}\left(u_{\mathrm{i}}i_{\mathrm{fi}}^* - u_{\mathrm{inj}}i_{\mathrm{fo}}^*\right)$ is a feedforward item, k_{p} and k_{i} are the proportional and integral coefficient, respectively, which should be less than zero to ensure the stability. Then, according to Table 3,

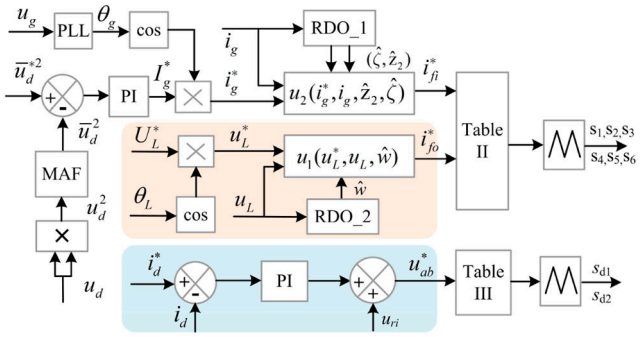

Fig. 4 *Overall control block diagram of the proposed scheme*

the duty ratios of the switches in the de-coupling circuit are obtained. The control block is shown in Fig. 4.

5 Parameters design

Input filter C_i and L_p: The first step is to determine the capacitance of the filter capacitor C_i. Based on the constraint of the capacitor voltage ripple, the following limit is obtained:

$$C_i \geq \frac{i_p - I_{dc}}{\Delta v_1 f_s} \frac{i_{fi}^*}{I_{dc}} \tag{40}$$

where Δv_1 is the allowable voltage ripple and I_{dc} is the dc-link current in steady-state.

The next step is to determine the inductor L_p. Assume the cut-off frequency of the input filter is f_c ($f_c \in (0.1-0.5)f_s$), then

$$L_p \geq \frac{1}{4\pi^2 f_c^2 C_f}. \tag{41}$$

Based on (40) and (41) and considering some design margin, C_i and L_p are selected.

Out filter capacitor C_{inj}: Similarly, based on the capacitor voltage ripple, the following limit is obtained:

$$C_{inj} \geq \frac{I_{dc} - i_L}{\Delta v_2 f_s} \frac{i_{fo}^*}{I_{dc}} \tag{42}$$

where Δv_2 is the allowable voltage ripple.

Decoupling capacitor C_d: According to (23), u_d can be solved out and expressed as

$$u_d = \sqrt{\int \frac{2(p_{in} - p_{out})}{C_d} + \bar{u}_d}. \tag{43}$$

Clearly, a larger $\bar{u}_d$ will lead to larger voltage stress; while, a smaller $\bar{u}_d$ will lead to a larger C_d to let (43) make sense. The way in [27] to determine the values of C_d and $\bar{u}_d$ is adopted. As a trade-off between the cost and voltage stress, C_d and $\bar{u}_d$ are selected to be 100 μF and 160 V.

As for the dc-link filter inductor L_d, maintaining the dc-link current ripple inside an acceptable range is the main consideration. The current ripple is related to the switching frequency, switching pattern, duty ratios, and voltages across the inductor besides the value of the dc-link filter inductor. Unfortunately, the analytical expression of the maximum current ripple is hard to solve. The reasons are (i) complex loci of the current sector $\boldsymbol{I}_{ref}$ and (ii) time-varying voltages (u_{inj}, u_i, u_d) across the dc-link inductor. In practice, the value of the dc-link inductor is determined based on the simulation results.

6 Simulations and experimental results

The simulation experiment and physical experiment have been both conducted to verify the effectiveness of the proposed UPQC.

Table 4 Parameters used in simulation and experiment

Parameters	Symbol	Value
rated source voltage	u_g/f_g	110 V_{rms}/50 Hz
input filters	L_p/C_i	0.6 mH/10 μF
intermediate inductor	L_d	2 mH
decoupling capacitor	C_d	100 μF
output filters	C_{inj}	15 μF
linear load_1	R/C	25 Ω/100 μF
linear load_2	R/L	25 Ω/50 mH
non-linear load composed by diode bridge rectifier	R/L/C	50 Ω/25 mH/120 μF
switching frequency	f_s	20 kHz
load voltage	u_L	110 V_{rms}/50 Hz

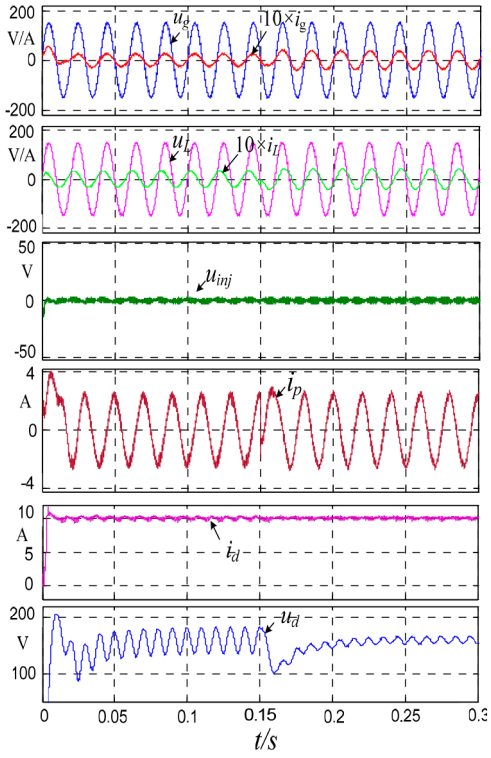

Fig. 5 *Simulation results of reactive power compensation and the waveforms from the top to the bottom are the grid voltage/ current (u_g/i_g), the output voltage/current (u_L/i_L), the series compensation voltage u_{inj}, the compensation current i_p, the dc-link inductor current (i_d), and the buffering capacitor voltage (u_d)*

The simulation experiment is conducted in MATLAB/SIMULINK environment, and the physical experiment is carried out on a built prototype in the Lab.

The experimental parameters are the same in both cases and listed in Table 4. The reference values of $\bar{u}_d^*$ and i_d^* are 160 V and 10 A, respectively. The simulation waveforms are obtained by using the Simulink Scope block and the experimental waveforms are captured by using the oscilloscope Tektronix MDO3014.

6.1 Simulation results

Fig. 5 shows the simulation results for reactive power compensation with a linear load. Initially, a capacitive load (Linear load_1 and the load impedance is $Z_c = 40.5\angle -52°$) is adopted and the load current i_L leads the load voltage u_L by 52°. At $t = 0.15$ s, the load is switched to an inductive load (Linear load_2 and the load impedance is $Z_L = 29.5\angle 32°$) and the load current i_L lags the load voltage u_L by 32°. During the entire process, the source current i_g keeps always sinusoidal and in phase with the source

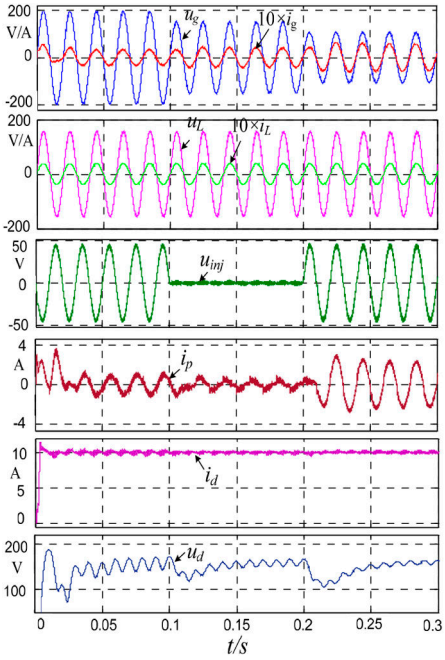

Fig. 6 *Simulation results of voltage sag/swell compensation and the waveforms from the top to the bottom are the grid voltage/current (u_g/i_g), the output voltage/current (u_L/i_L), the series compensation voltage u_{inj}, the compensation current i_p, the dc-link inductor current (i_d), and the buffering capacitor voltage (u_d)*

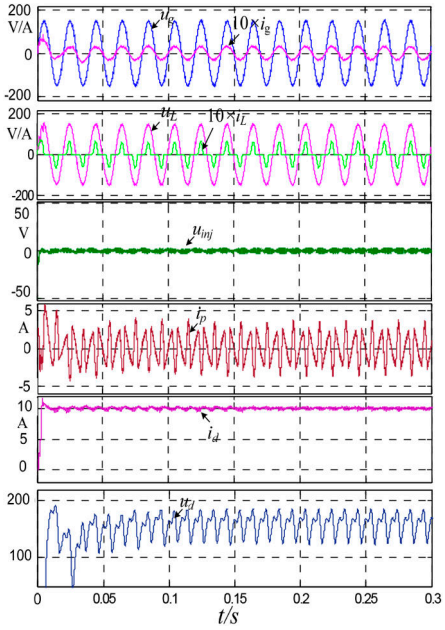

Fig. 7 *Simulation results of load current harmonics compensation and the waveforms from the top to the bottom are the grid voltage/current (u_g/i_g), the output voltage/current (u_L/i_L), the series compensation voltage u_{inj}, the compensation current i_p, the dc-link inductor current (i_d), and the buffering capacitor voltage (u_d)*

voltage u_g because of the compensation current i_p provided by the UPQC. This confirms that the UPQC shows a good performance in terms of reactive power compensation. In this case, u_{inj} is equal to zero due to the fact that no compensation voltage is required.

Fig. 6 shows the voltage compensation performance of the UPQC. As seen, a 30% voltage swell occurs at source voltage in the interval [0–0.1 s] and a 30% voltage sag occurs in the interval [0.2–0.3 s]. As expected, the u_{inj} is out of (in) phase with grid voltage u_g with the same amplitude of 46.8 V when the grid voltage swell (sag) occurs. Therefore, the load voltage is always kept at the desired value. Meanwhile, the source current i_g is synchronised with the source voltage u_g over the entire period, which indicates that the unity power factor is achieved.

Fig. 7 shows the steady-state performance of UPQC in terms of harmonic compensation. As seen, the current i_L is seriously distorted due to the non-linear diode rectification load. However, the grid current i_g is sinusoidal and in the phase of u_g because the reactive and harmonic currents are compensated by current i_p. Therefore, the converter demonstrates excellent harmonic current compensation ability under the proposed direct control method.

Fig. 8 shows the simulation results when current and voltage sag compensations are considered at the same time. A 30% voltage sag occurs throughout the whole process. However, the load voltage is always 110 V_{rms} due to the sag voltage compensation. Before $t = 0.1$ s, an inductive load is connected and the load current i_L lags the load voltage u_L. Also, after $t = 0.1$ s, a diode rectifier non-linear load is connected and the load current i_L is distorted

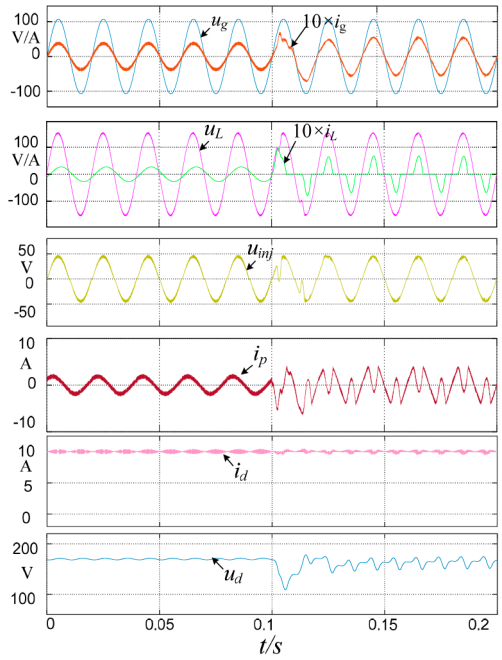

Fig. 8 *Simulation results when compensating the current harmonics and voltage sag at the same time, the waveforms from the top to the bottom are the grid voltage/ current (u_g/i_g), the output voltage/current (u_L/i_L), the series compensation voltage u_{inj}, the compensation current i_p, the dc-link inductor current (i_d), and the buffering capacitor voltage (u_d)*

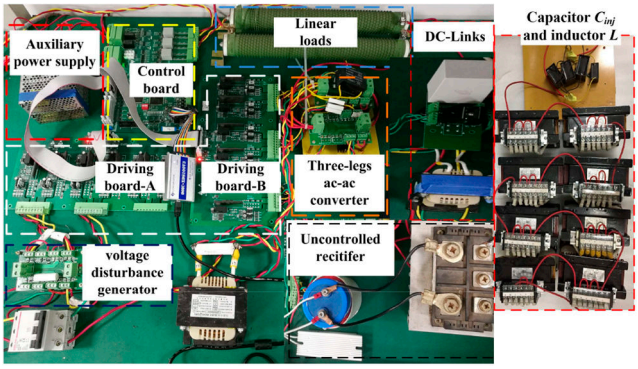

Fig. 9 *Experimental set-up of the UPQC*

seriously. However, the grid current is always in phase with the grid voltage due to current compensation.

From Figs. 5–8, it can be found that the inductor current i_d is always controlled to be constant (with only switching frequency ripple). This is because the capacitor voltage u_d swings to buffer the reactive power. For example, in Fig. 7, u_d fluctuates between 125 and 180 V to absorb and release power periodically due to exchanging ripple power with the grid side (generating a desired compensation current i_L). Although large fluctuations exist in the capacitor voltage u_d, the performance of the UPQC is satisfactory. The reason is that the performances of the UPQC are directly dependent on inductor current i_d.

6.2 Experimental results

A prototype has been built for experimental verification, which is shown in Fig. 9. The setup includes a three-leg ac-ac converter, driving boards A and B, an auxiliary power supply, a control board (with a signal processor TMS320F28335), a voltage disturbance generator and a dc-link (comprising a dc inductor and power buffer circuits). Parameters of the experiment are the same as those in the simulation. To demonstrate the feasibility of the proposed topology and control scheme, three sets of experiments are carried out and the corresponding experimental results are shown in Figs. 10–19.

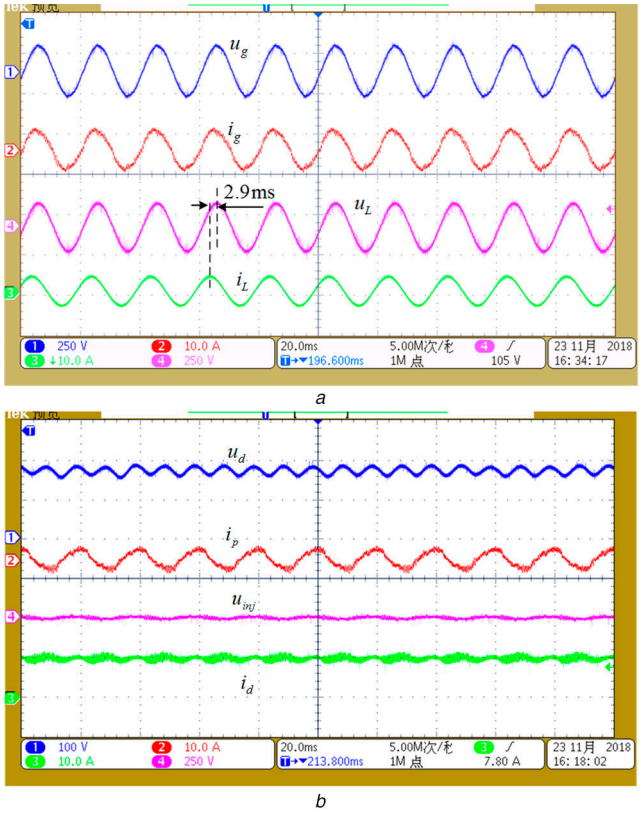

Fig. 10 *Experimental results for reactive power compensation with the capacitive load*

(a) Waveforms of the grid voltage/current (u_g/i_g) and the output voltage/current (u_L/i_L), ***(b)*** Waveforms of the buffering capacitor voltage (u_d), the compensation current (i_p), the series compensation voltage (u_{inj}), and the dc-link inductor current (i_d)

The experimental data are sampled by using the current probe (voltage probe) Tektronix THDP0200 (Tektronix TCP0020).

To verify the capability of compensating reactive power of the UPQC, two kinds of tests, respectively, with capacitive and inductive loads have been carried out. Fig. 10 shows the experimental results with the capacitive load. The source and load voltage/current waveforms are shown in Fig. 10*a*. As seen, the load current i_L leads u_L by about 2.9 ms (52°). However, the source current i_g is in phase with the source voltage u_g due to the compensation current i_p, which is generated by the UPQC. Fig. 10*b* shows the waveforms of the capacitor voltage u_d, the reactive power compensation current i_p, the injection voltage u_{inj}, and the dc-link inductor current i_d, from top to bottom. Fig. 11 shows the waveforms under the case of the inductive load. As seen, the load current i_L lags u_L by about 1.8 ms (32°) and the source current i_g is still in phase with the source voltage u_g. In both cases, the experimental results coincide with those in the simulations.

Figs. 12 and 13 show the total harmonic distortion (THD) and spectra analysis of the source voltage u_g, source current i_g, load voltage u_L and load current i_L under the scenario of capacitive and inductive loads. As seen, the THDs of the grid current are 3.08 and 3.88%, respectively, which is <5%. Besides, the load voltage and current have a very low THD, which verifies the effectiveness of the proposed control method.

Fig. 14/15 shows the waveforms under a 30% depth of the grid voltage sag/swell. The disturbance happens at $t = T$. It can be found that the amplitude of u_L remains constant despite the variations of the source voltage due to the compensation voltage u_{inj}. Note that no spike or collapse happens to the source current i_g during the transient process. The power difference is temporarily supported by the dc-link. Therefore, a drop (rise) of the capacitor voltage u_d could be found in Fig. 14*b* (Fig. 15*b*).

The total harmonic distortions (THDs) of the source and load currents/voltages during the voltage sag (swell) are shown in

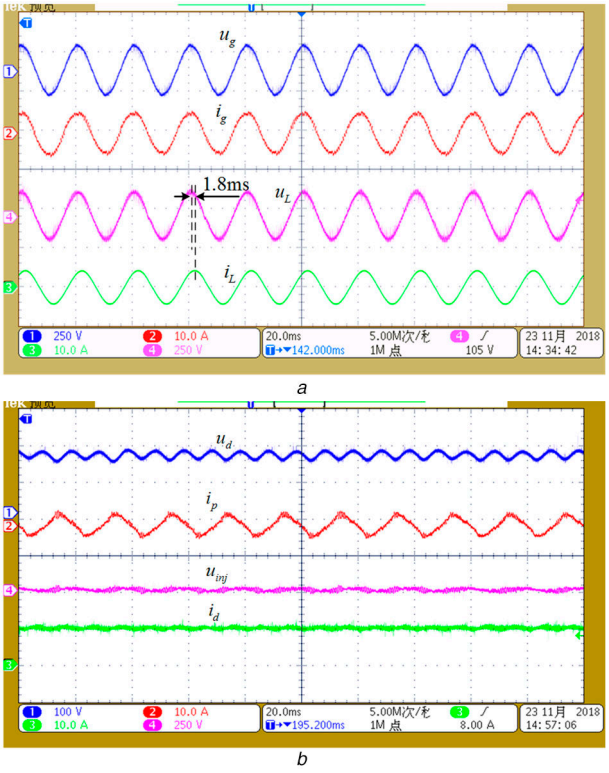

Fig. 11 *Experimental results for reactive power compensation with the capacitive load*

(a) Waveforms of the grid voltage/current (u_g/i_g) and the output voltage/current (u_L/i_L), ***(b)*** Waveforms of the buffering capacitor voltage (u_d), the compensation current (i_p), the series compensation voltage (u_{inj}), and the dc-link inductor current (i_d)

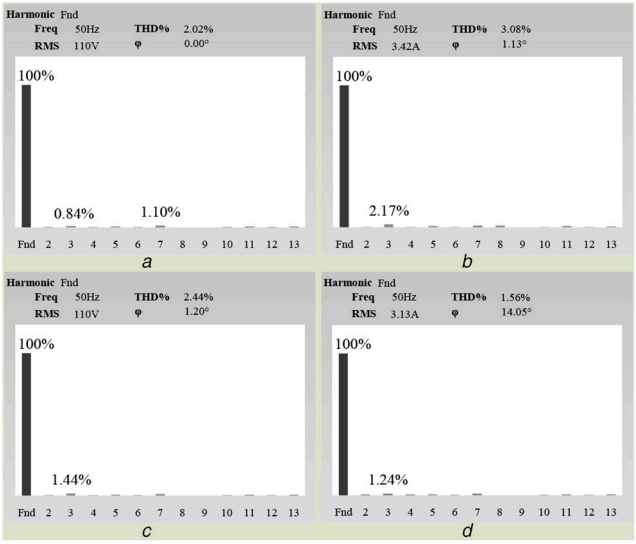

Fig. 12 *Spectral analysis of the experimental results for reactive power compensation with the inductive load*

(a) Source voltage u_g, ***(b)*** Source current i_g, ***(c)*** Load voltage u_L, ***(d)*** Load current i_L

Fig. 16/Fig. 17. As seen, the THD of load voltage u_L is <1.5%. What is more, high-quality source current i_g is always kept with low THD and odd harmonics.

Fig. 18 shows the steady-state waveforms when a non-linear load is connected. In Fig. 18*a*, the source current i_g is sinusoidal and synchronised with source voltage u_g, while the load current i_L is severely distorted. The measured THDs of the source current and the load current are 4.74 and 82.5%, respectively, as seen in Fig. 18. Therefore, the UPQC shows a good performance in mitigating the harmonic currents due to the non-linear loads. What is more, the load voltage is also well regulated with the THD of

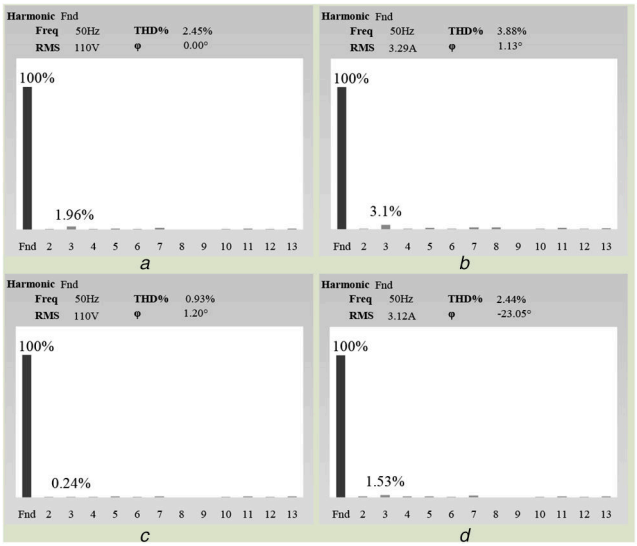

Fig. 13 *Spectral analysis of the experimental results for reactive power compensation with the capacitive load*

(a) Source voltage u_g, ***(b)*** Source current i_g, ***(c)*** Load voltage u_L, ***(d)*** Load current i_L

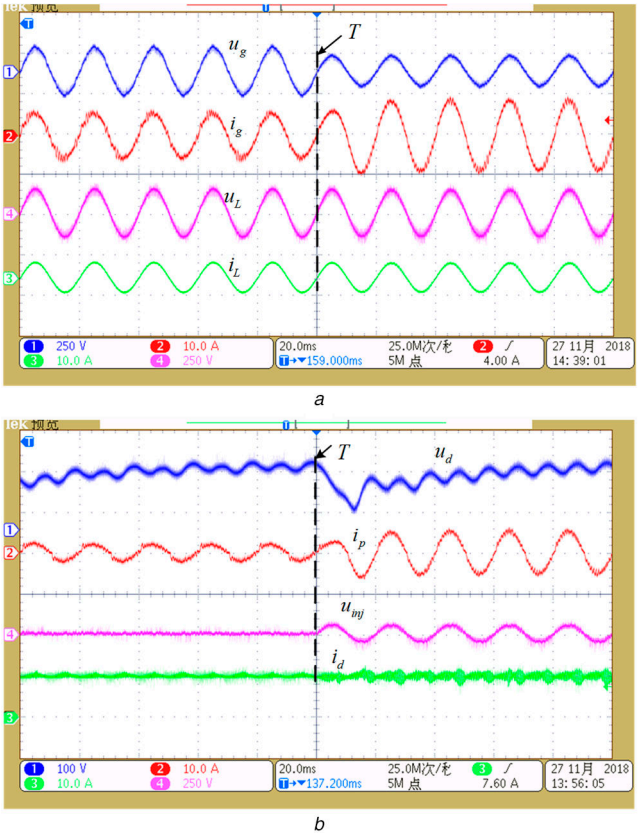

Fig. 14 *Experimental results for voltage sag compensation*

(a) Waveforms of the grid voltage/current (u_g/i_g) and the output voltage/current (u_L/i_L), ***(b)*** Waveforms of the buffering capacitor voltage (u_d), the compensation current (i_p), the series compensation voltage (u_{inj}), and the dc-link inductor current (i_d)

1.89%. The waveforms in Fig. 18*b* are the capacitor voltage u_d, the harmonic compensation current i_p, the injection voltage u_{inj}, and the dc-link current i_d, from top to bottom. The dc-link current approximately remains constant, while the capacitor voltage u_d swings around its reference value due to the power difference between the source and load is buffered in the decoupling capacitor. The experimental results are in accordance with those in the simulations.

Table 5 shows comparisons of the number of switching legs required, the use of isolation transformer, the existence of

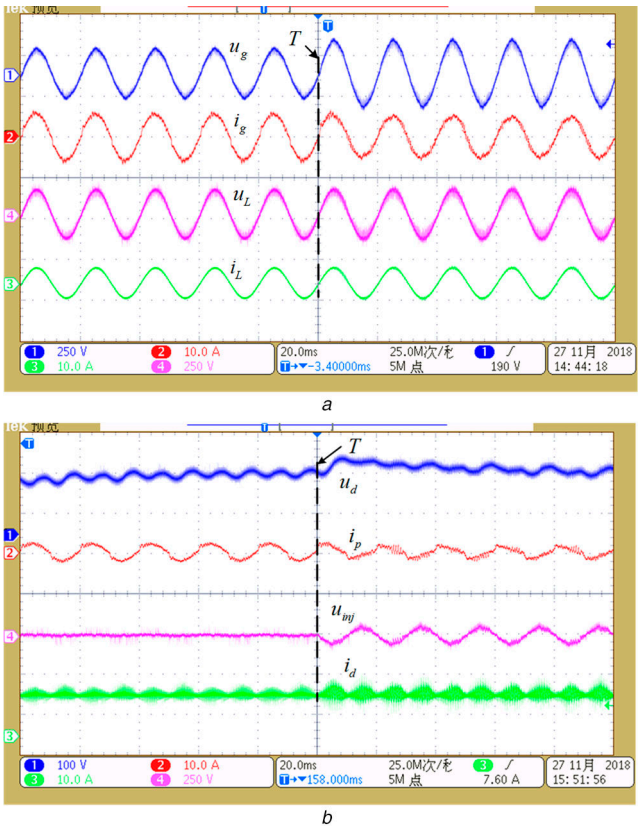

Fig. 15 *Experimental results for voltage swell compensation*

(a) Waveforms of the grid voltage/current (u_g/i_g) and the output voltage/current (u_L/i_L), ***(b)*** Waveforms of the buffering capacitor voltage (u_d), the compensation current (i_p), the series compensation voltage (u_{inj}), and the dc-link inductor current (i_d)

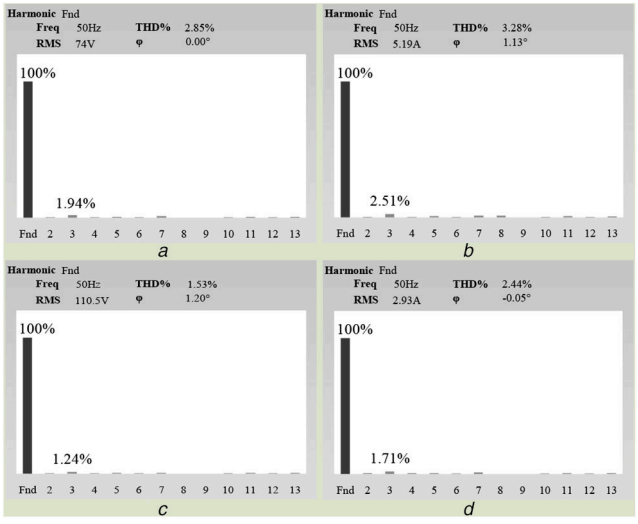

Fig. 16 *Spectral analysis of the experimental results for voltage sag compensation*

(a) Source voltage u_g, ***(b)*** Source current i_g, ***(c)*** Load voltage u_L, ***(d)*** Load current i_L

circulating current, passive components in the dc-link, voltage stress, and the power rating. Except for the usage of switching legs, the proposed UPQC shows comparable performances in the other aspects. For the proposed UPQC, the voltage stresses of switches S_5 and S_6 are increased under the case of voltage sag/swell as the injected voltage u_{inj} is not equal to zero any more. For other topologies, the voltage stresses are always the dc-link voltage in spite of the operation cases. Note that all the other UPQCs need bulky electrolytic capacitors (E-caps) to obtain a stiff dc-link voltage; while, in the proposed one, only passive components with small values are needed, which is beneficial for reducing the size and improve lifetime (no E-caps).

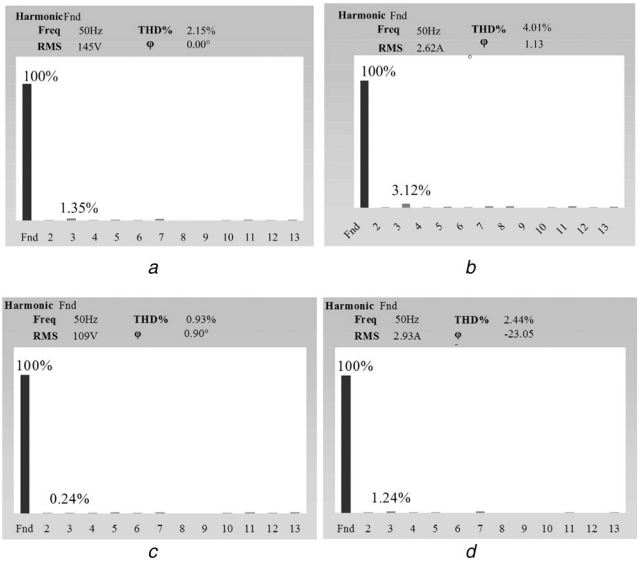

Fig. 17 *Spectral analysis of the experimental results for voltage swell compensation*

(a) Source voltage u_g, ***(b)*** Source current i_g, ***(c)*** Load voltage u_L, ***(d)*** Load current i_L

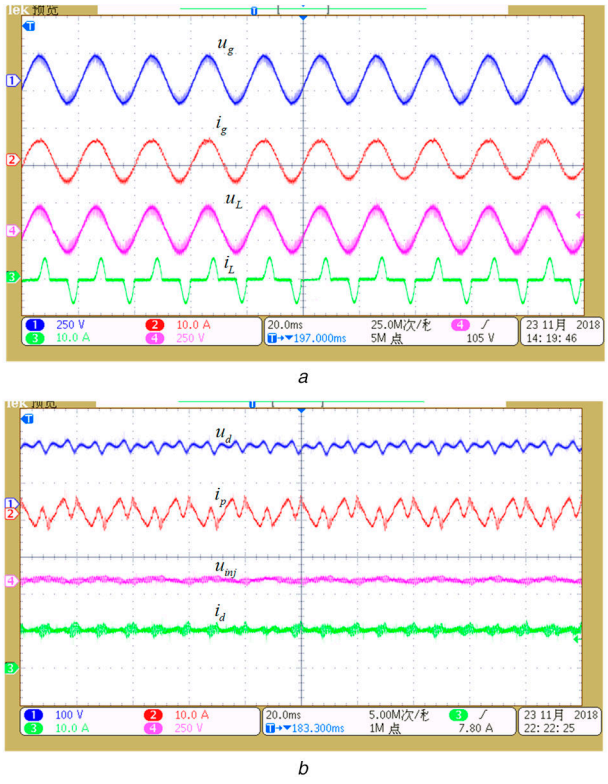

Fig. 18 *Experimental results for current harmonics compensation*

(a) Waveforms of the grid voltage/current (u_g/i_g) and the output voltage/current (u_L/i_L), ***(b)*** Waveforms of the buffering capacitor voltage (u_d), the compensation current (i_p), the series compensation voltage (u_{inj}), and the dc-link inductor current (i_d)

7 Conclusion

This study presents a unified current-source PQ conditioner of inherent no circulating current. Owing to the absence of a bulky inductor and isolation transformer, it has the benefits of compact structure and high power density. Since there is no circulating current issue in this topology, it is easier to design the controller of the system. In addition, a direct control method based on ERDO is proposed to control both the source current and load voltage of the conditioner, which achieves good tracking performance without harmonic extractors. Both simulation and experimental results have verified the feasibility and effectiveness of the proposed UPQC and control method.

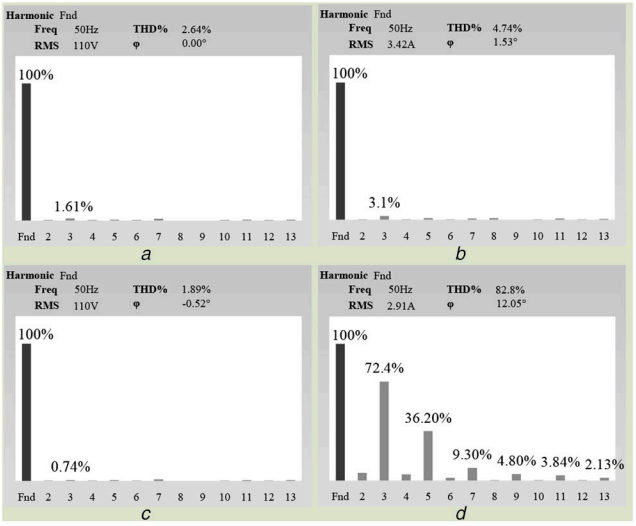

Fig. 19 *Spectral analysis of the experimental results for current harmonics compensation*
(a) Source voltage u_g, ***(b)*** Source current i_g, ***(c)*** Load voltage u_L, ***(d)*** Load current i_L

Table 5 Comparison of the proposed UPQC with other single-phase UPQCs

Configuration	No. of switching legs	Isolation transformer	Circulating current	Dc-link	Voltage stress of switching legs	Power rating
ref. [9]	four	yes	no	bulky capacitor (1100 μF)	DC-link voltage V_{dc} (115 V)	127 VA
ref. [10]	four	yes	no	bulky capacitor (2200 μF)	DC-link voltage V_{dc} (300 V)	50 kVA
ref. [11]	four	yes	no	bulky capacitor (5000 μF)	DC-link voltage V_{dc} (500 V)	—
ref. [13]	four	no	yes	bulky capacitor (2200 μF)	DC-link voltage V_{dc} (250 V)	1.2 kVA
ref. [15]	three	no	no	bulky capacitor (4700 μF)	DC-link voltage V_{dc} (230 V)	1 kVA
ref. [16]	two	yes	no	two bulky capacitors (−)	DC-link voltage V_{dc} (300 V)	1 kVA
ref. [18]	two	no	no	two bulky capacitors (1000 μF)	DC-link voltage V_{dc} (400 V)	1 kVA
ref. [23]	four	yes	no	bulky capacitor (2000 μF)	DC-link voltage V_{dc} (−)	200 VA
proposed UPQC	three	no	no	small capacitor and small inductor (100 μF, 2 mH)	u_g@S_1 and S_2, u_{inj}@ S_5 and S_6, max(u_g, u_{inj}) @ S_3 and S_4,	218 VA

8 Acknowledgments

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